REMARKS

This is intended as a full and complete response to the Office Action dated March 1, 2004, having a shortened statutory period for response set to expire on June 1, 2004. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-24 remain pending in the application and are shown above. Claims 25-31 stand withdrawn by the Examiner. Claims 1 and 7-15 stand rejected, and claims 2-6 and 16-24 are indicated to be allowable by the Examiner. Reconsideration of the rejected claims is requested for reasons presented below.

Claim 1 has been amended to clarify aspects of the claimed invention. Claim 2 is amended to be in independent form.

Claims 1 and 7-15 stand rejected under 35 USC § 103(a) in view of Aegerter et al. (US 6,632,292) on grounds that it would have been obvious to provide an annealing station in the Aegerter et al. plating system as an additional complementary station to facilitate adherence or bonding of the metal to the substrate. The examiner further stated that it would have been obvious to add an annealing or CMP station to a wafer plating system as a complimentary processing station for its known benefit of enhancement of bonding of metal to the wafer. Applicant respectfully traverses the rejection.

The reference does not teach the combination of an anneal chamber, a substrate activation chamber, an electroless plating chamber, and a spin rinse dry chamber, all in communication with a common central substrate transfer enclosure, as claimed, nor would it be obvious to combine such chambers onto a single platform as asserted by the Examiner. Aegerter et al. discloses at col. 16, lines 30-65 and in Figures 14 and 15, a processing tool for the electro deposition of a metal such as copper in which additional processing stations may be included such as a pre-wetting station, a clean dry station, etc. The examiner further notes that Aegerter et al. is silent concerning the inclusion of an annealing station, asserting however, that such would have been obvious because it

was known in the art to provide for annealing or CMP of a metal plated wafer in order to facilitate adherence or bonding of the metal to the wafer.

In the discussion of the background for the invention in Aegerter et al., an electro deposition process is described in which a different problem is encountered in the further processing of a wafer during annealing or CMP. The described process begins with the deposition of a first barrier layer onto a wafer, and then a thin film layer, which may be deposited by PVD to serve as a seed layer for the subsequent electroplating of a further metal layer such as copper. (Col 1, lines 56-60). The reference notes that in these pre electro deposition processes, copper will be deposited onto the wafer bevel, in many cases the deposited copper non-adherent, and subject to flaking off in subsequent processing steps such as annealing or CMP. Aegerter et al. goes on to note that because the electroplated layers are deposited with an edge exclusion, the previously deposited seed layers are left exposed, and subject to flaking during post processing.

By the present invention, a completely different problem is addressed. As device sizes become smaller and smaller, and aspect ratios increased, it becomes more and more difficult to deposit both barrier and copper seed layers without defects or holes. [paragraph 0004]. To address this problem, applicants have developed a process and a tool for carrying out an electroless process where annealing can occur by integrating the activation, electroless deposition, and anneal steps within the same tool, better processing and higher throughput is also facilitated.

It is generally known, as evidenced by Aegerter et al., to anneal an electroplated copper film to stabilize it and improve conductivity. However, contrary to the examiner's assertion, there is nothing in the reference to suggest anneal within a process tool comprising an electroless substrate plating chamber.

Thus, Aegeter et al: fails to teach or suggest the combination of chambers in a unitary apparatus including a substrate activation chamber, an electroless plating chamber, a spin rinse chamber, and a substrate anneal chamber.

It is, thus, respectfully submitted that Aegerter et al. fails to teach, show or suggest a semiconductor processing apparatus, as recited in claim 1. Withdrawal of the rejection is respectfully requested.

Applicant further traverses the rejection of dependent claims 7-15 on grounds that claim 1 as now amended is in allowable form. Withdrawal of the rejection of claims 1 and 7-15 is respectfully requested.

Claim 2 is amended to include all limitations of allowable dependent claim 2. Thus, claim 2 and dependant claims 3-6 are now likewise allowable.

The Examiner indicated claims 16-24 are objected to but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Directing the Examiner's attention to claim 16, as an independent claim, it is believed that it is already in condition for allowance as it contains all of the key elements cited by the examiner, which if claimed in combination, would render the claim allowable. Accordingly, it is submitted, that claim 16 as presented is allowable and that claims 17-24, being dependant upon an allowable claim, are likewise allowable.

In conclusion, the reference cited by the Examiner does not teach, show or suggest the invention as claimed.

The Examiner's request for copies of the non patent literature references has been noted, and copies are included in a Supplemental Information Disclosure Statement filed with this response.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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